Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated October 21, 2005, indicated that claims 1-9 are rejected under 35 U.S.C. § 103(a) over Larky *et al.* (U.S. Patent No. 6,311,294) in view of Watson *et al.* (U.S. Patent No. 6,218,969).

Applicant has amended claim 1 to characterize the bus interface to more explicitly state that which was already implicit. The amendment does not introduce new matter as support for these changes may be found, for example, at page 3, lines 1-9 of the instant Specification. The claim is believed to be patentable over the cited references for the reasons presented below.

Applicant respectfully traverses the new ground of rejection (under Section 103(a)) because the Office Action still fails to present a combination of references that corresponds to several of the claimed limitations. As the new ground of rejection still relies primarily on the '294 reference of the previous rejections, Applicant maintains the previous arguments based upon deficiencies of the '294 reference. Moreover, Applicant notes that the Examiner has reversed the assertion that the '294 reference does not teach a FIFO by now asserting (without further explanation or support) that logical data pipe 34 implies FIFO (at page 2 of the Office Action). However, this assertion is not supported by the '294 reference, which teaches, via Fig. 3, that logical data pipe 34 is an interface for accessing data between a host buffer and a USB device software client. Such a software interface does not imply the limitations of the claimed FIFO buffer. Thus, the Examiner's unsupported assertion fails to overcome this deficiency of the '294 reference.

In addition to the above, the Office Action still fails to show that the '294 reference teaches a FIFO buffer, as claimed, because the memory buffer asserted in the Office Action does not correspond to the claimed FIFO buffer. For example, Applicant submits that memory block 32 of Fig. 3 is located in the host device, not the USB device.

The Examiner acknowledges in the new ground of rejection at page 3 that the '294 reference fails to teach a situation where the bus interface determines to send interrupts to the processor as a function of whether the FIFO buffer is empty and whether interrupts have

yet been generated since the processor has written into the buffer. In an attempt to overcome this deficiency, the Examiner proposes modifying the '294 device (without presenting any evidence or explanation of how the combination would be implemented) to include handling interrupts as taught by the '969 reference. The '969 reference is directed to a signal converter for interconnection between a USB and parallel port protocols. While the Office Action asserts that the '969 reference teaches a bus interface for sending interrupts to the processor, Applicant fails to recognize any mention of a bus interface sending an interrupt to a processor. Instead, the cited passages teach responding to interrupt requests from the host and sending a nACK or data to the host. *See, e.g.,* column 7, lines 48-51.

Moreover, the '969 reference does not teach that any interrupt decisions are made based upon the state of a FIFO buffer. Applicant fails to see the relevance of the Office Action's assertion that the '969 reference teaches that a decision is made in regards to memory buffer 16 of Fig. 1 because: 1) memory buffer 16 is not a FIFO buffer (*see, e.g.,* column 5, lines 32-38) and 2) memory buffer 16 is not used in correlation to sending an interrupt to a processor. Thus, the proposed combination fails to correspond, at least, to the claimed bus interface.

Further, the newly cited combination of references still fails to teach a first station that repeatedly sends requests for data to a second station and also fails to teach a second station that responds to each request by sending a message with a data item or sending a negative acknowledge signal, as claimed, in view of the previously argued deficiencies of the '294 reference. The Office Action cites portions of the Background section of the '294 disclosure (pending-IN process) as allegedly corresponding to these claimed aspects; however, the '294 disclosure teaches that the cited host 12 and device 14 operate using an alternative process that intentionally avoids these claim limitations and expressly teaches away from the claimed invention. *See* column 5, lines 20-26 and line 67 – column 6, line 12. The relied upon embodiment of the '294 reference does not operate in accordance with the cited teachings of the reference's background section; therefore, the proposed modification (which does not address this deficiency) of the relied upon '294 embodiment fails to correspond to the claimed invention.

Without a showing of correspondence to each of the claimed limitations, the Section 103(a) rejection cannot be maintained, and Applicant accordingly requests that the rejection be withdrawn.

Applicant also traverses the Section 103(a) rejection because the Office Action fails to present evidence of motivation that the skilled artisan would introduce a bus interface of the newly-cited '969 reference to the '294 teachings. The '969 reference teaches a USB to parallel port signal interface where the data is supplied by the peripheral device behind the parallel port. In contrast, the '294 reference teaches that the processor for supplying data and controlling the bulk data controller is located in the USB device. *See, e.g.*, column 5, lines 26-45. Thus, including the interface of the '969 reference as part of the cited embodiment of the '294 reference is neither motivated nor logical. Without presenting any evidence of motivation in the cited references to modify the '294 reference to achieve the claimed invention, the Office Action fails to present a *prima facie* Section 103(a) rejection and Applicant requests that the rejection be withdrawn.

Moreover, Applicant maintains that the primary reference cited by the Office Action teaches away from the claimed invention. The instant invention is directed to, for example, a bus system that includes a first station repeatedly sending requests for data to a second station and the second station responding to each request (*e.g.*, claim 1). The Office Action relies on a portion of the Background of the '294 reference (column 2, lines 36-48) as allegedly corresponding to these limitations. A further citation to the Summary (column 3, lines 18-38) teaches that the host 12 only sends IN tokens to the device after receipt of a data available signal, and the device can stop the host's sending of IN tokens by sending a dry signature signal. This ability to prevent the host from sending the IN tokens means that the host does not send the tokens repeatedly; instead it sends them merely upon initiation by the device. As discussed above, the '294 reference teaches away from these aspects. The '294 reference teaches an alternative system where the device 14 (alleged second station) initiates bulk data retrieval, which prevents the host 12 (alleged first station) from continuously sending IN tokens to the device 14. *See,* column 5, line 67 – column 6, line 12. The '294 system purposely avoids having the host repeatedly sending requests to the device in order to relieve inefficiencies such as traffic burden on the bus and degradation of overall system performance. *See, e.g.*, column 2, lines 49-62. Since the primary '294 reference teaches away from the claimed invention,

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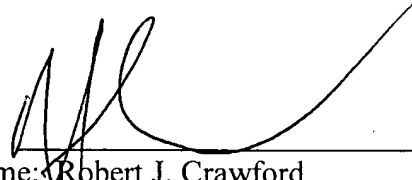the skilled artisan would not be motivated to modify the '294 reference as asserted. Applicant accordingly requests that the rejection be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Mr. Peter Zawilski, of Philips Corporation at (408) 474-9063.

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